Powerful Sensing Solutions for a Better Life

DTOS ACCELEROMETER

Digital Thermal Orientation Sensing Accelerometer

MXC6226XU

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Features

- **Fully Integrated Thermal Accelerometer**
- **X/Y Axis, 8 bit, Acceleration A/D Output (± 2g)**
- **Absolute 0G offset less than +/- 50mg**
- **4-position Orientation Detection**
- **Shake Detection with Interrupt**
- **Programmable Shake Threshold**
- **Shake Direction Detection**
- **I^2C Interface**
- **Power Down Mode**
- **Shock Survival Greater than 50,000 g**
- **Operating Supply Voltage from 2.5V to 5.5V with 1.8V compatible I/O**
- **Produces no Mechanical Sounds ("click")**
- **Package Size 3x3x1mm**

Applications

- **Consumer:**
  - Cell Phones
  - Digital Still Cameras (DSC)
  - Digital Video Cameras (DVC)
  - LCD TV
  - Toys
  - MP3, MP4 Players
- **Household Safety:**
  - Fan Heaters
  - Halogen Lamps
  - Iron
  - Cooling Fans

General Description

The MEMSIC Digital Thermal Orientation Sensor (DTOS) is the world's first fully-integrated orientation sensor. Its operation is based on our patented MEMS-thermal technology and is built using a standard 0.18um CMOS process. DTOS contains no moving parts (such as a ball) and thus eliminates field-reliability and repeatability issues associated with competitive products. It also eliminates the "click" sounds typically heard in ball based orientation sensors. Shock survival is greater than 50,000g. DTOS detects four orientations, shake and shake direction. In addition, it provides X/Y axis acceleration signals with very low 0g offset. An I^2C interface is used to communicate with this device and an interrupt pin (INT) is provided for shake and orientation. The DTOS also has a power down enabled through the I^2C interface.

Functional Block Diagram

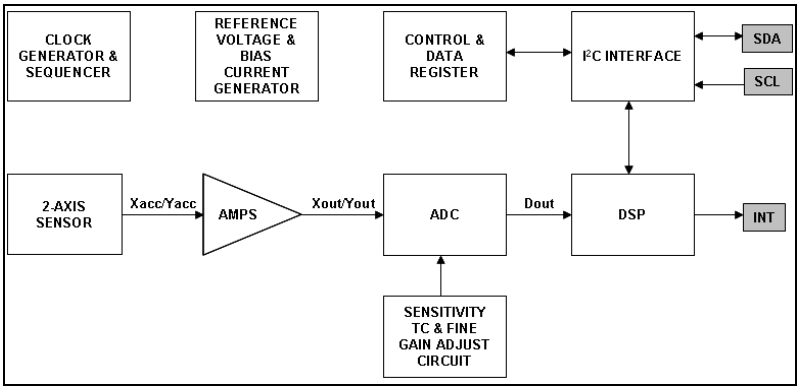

Figure 1

The DTOS is packaged in a hermetically sealed 6-pin surface mount package (3 mm x 3 mm x 1mm); the product is RoHS compatible and operates over -20~70℃ temperature range.

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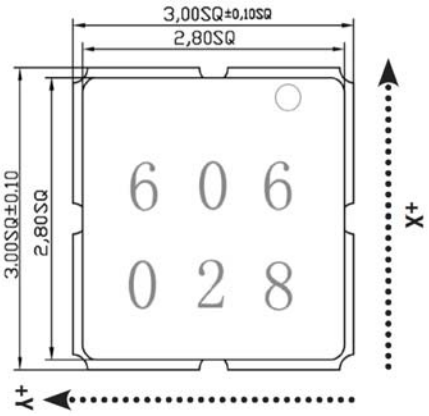

Figure 2

Top View

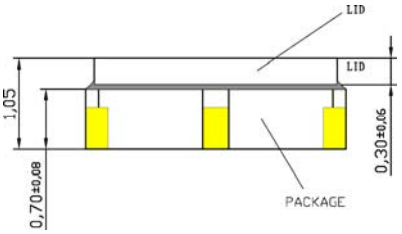

Figure 3

Side View

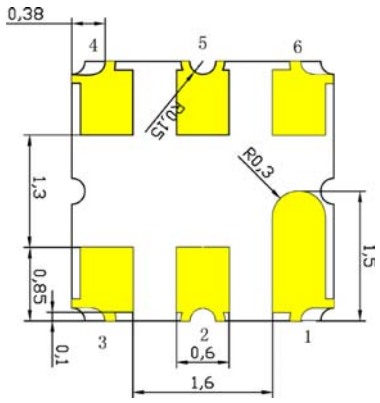

Figure 4

Bottom View

LCC6 Package Drawing Package Thickness:

1.05mm +/- 0.1mm

Pin Description: LCC6 Package

Pin	Name	Description
1	INT	This pin is the DTOS interrupt output. The logic level on this pin reflects the state of the INT bit in the STATUS register. INT is set when the orientation differs from the last orientation read by the processor, or a shake event is detected. INT is cleared upon reading of the STATUS register.
2	NC	During normal operation, this pin must be left floating.
3	VDD	This is the power supply input. The DC voltage should be between 2.5 and 5.5 volts.
4	I^2C SCL	This pin is the serial clock line for the I^2C interface. Since the DTOS only operates as a slave device, this pin is always an input.
5	I^2C SDA	This pin is the serial data line for the I^2C interface. It is an I/O pin that functions as an input during a write, and an output during a read from the DTOS.
6	GND	This is the ground pin for the DTOS.

Absolute Maximum Ratings*

Supply Voltage (V_{DD}) ……..-0.5 V to +7.0V
Storage Temperature ……..-40°C to +150°C
Acceleration ……..50,000 *g*

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications[1]

Parameter (Units)	Conditions	Minimum	Typical	Maximum
Operating Voltage Range (V)		2.5		5.5
VIO(I^2C interface)(V)		1.62	1.8	VDD
Supply Current (mA)	In power-up mode		1.2	
	In power-down mode		0.0004	0.001
Turn-On Time (ms)[2]			300	500
Turn-off Time (ms)				0.5
Operating Temperature Range (℃)		-20		+70
VDD Rise Time (ms)[3]				10

Notes: *1* All specifications are at 3V and room temperature unless otherwise noted. *2* Time to obtain valid data after existing power-down mode. *3* Maximum allowable power supply rise time from 0.25V to 2.5V (minimum). Slower VDD rise time may cause erroneous data retrieval from OTP memory at power-up.

Sensor Characteristics[1]

Parameter (Units)	Conditions	Minimum	Typical	Maximum
Measurement Range (g)	X/Y Axis			± 2.0
Alignment Error (°)	X/Y Axis		± 1.0	± 2.0
Sensitivity Error (%)	X/Y Axis	-5	0	5
Sensitivity (LSB/g)	X/Y Axis		64	
Sensitivity Drift Over Temperature (%)	Delta from 25 ℃ (-20 ℃ - 70 ℃)		± 12	± 18
Zero g Offset Bias Level (mg)	X/Y Axis (25 ℃)	-30		+30
Zero g Offset Temperature coefficient (mg/℃)	X/Y Axis (-20 ℃ - 70 ℃)		0.3	
3dB Signal Bandwidth (Hz)			10	

Notes: 1 All specifications are at 3V and room temperature unless otherwise noted.

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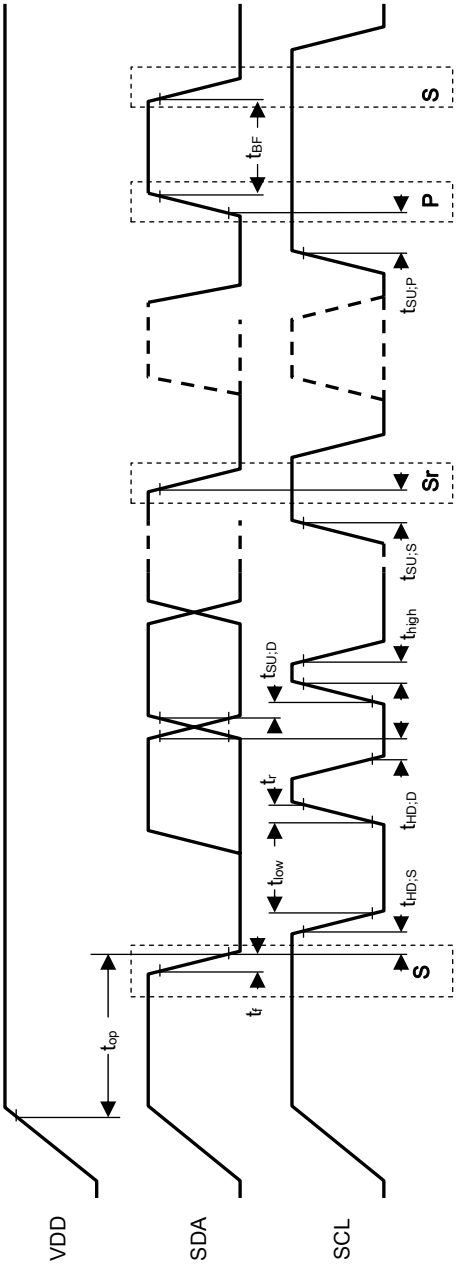

Figure 5

Digital Parameters

Symbol	Parameter (Units)	Minimum	Typical	Maximum
V_{IH}	High Level Input Voltage (Volts)	0.7*VIO		
V_{IL}	Low Level Input Voltage (Volts)			0.3*VIO
V_{HYS}	Hysteresis of Schmitt Trigger Input (Volts)	0.1		
I_{IL}	Input Leakage, All Inputs (uA)	-10		10
V_{OH}	High Level Output Voltage (Volts)	0.8*VIO		
V_{OL}	Low Level Output Voltage (Volts)			0.2*VIO

Digital Switching Characteristics

Symbol	Parameter (Units)	Minimum	Typical	Maximum
t_{op}	Operating Valid Time (ms)[1]	20		
f_{SCL}	SCK Clock Frequency (kHz)	0		400
t_r	Rise Time (us)			0.3
t_f	Fall Time (us)			0.3
t_{low}	SCL Low Time (us)	1.3		
t_{high}	SCL High Time (us)	0.6		
$t_{HD;D}$	Data Hold Time (us)	0		0.9
$t_{SU;D}$	Data Set-Up Time (us)	0.1		
$t_{SU;S}$	Start Set-Up Time (us)	0.6		
$t_{HD;S}$	Start Hold Time (us)	0.6		
$t_{SU;P}$	Stop Set-Up Time (us)	0.6		
t_{BF}	Bus Free Time Between Start and Stop (us)	1.3		

Notes: 1 Time to operate DTOS through I²C interface after power being supplied to VDD. 2. It is not recommended to keep both SCL and SDA signals low for over 10ms.

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Circuit Schematics

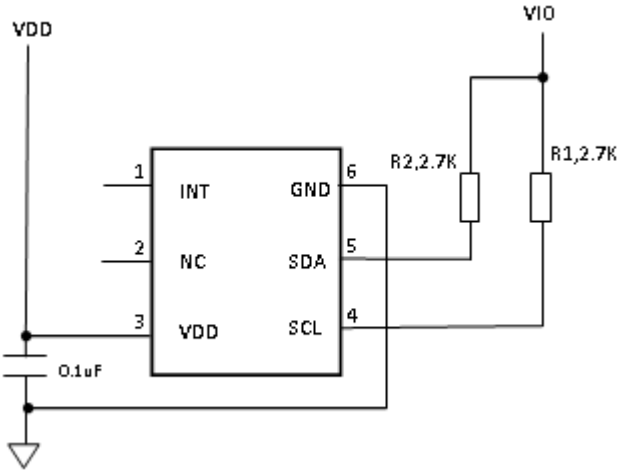

Figure 6

Note:

- R1 and R2 are pull-up resistors, the value can be determined by customer according to the requirement of the host device, and the recommendation value is 2.7KOhm.
- INT does not need any pull-up/pull-down resistor
- If INT is not used, keep it disconnected (don't pull up or pull down)
- Leave NC pin as no connection.

Landing Pattern (Unit: mm)

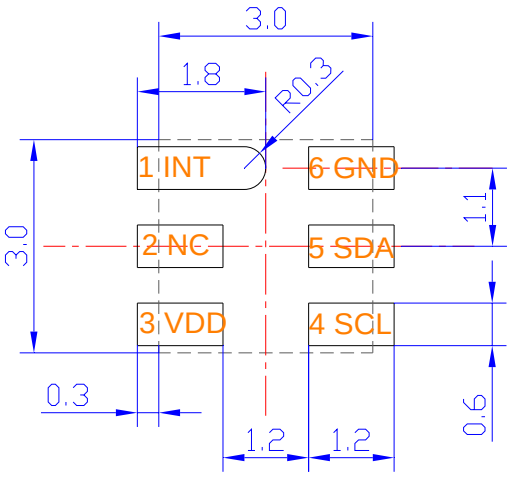

Figure 7

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Reflow Profile

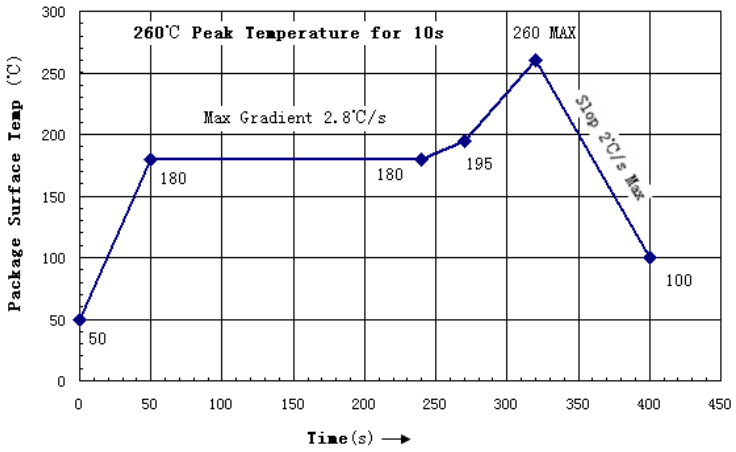

Figure 8

Reflow Profile

Note:

- Reflow is limited to two cycles.
- If a second reflow cycle is implemented, it should be applied only after device has cooled down to 25℃ (room temperature)
- Figure 8 is the reflow profile for Pb free process
- The peak temperature on the sensor surface must be limited to under 260℃ for 10 seconds.
- Follow solder paste supplier's recommendations for the best SMT quality.

Manual Soldering

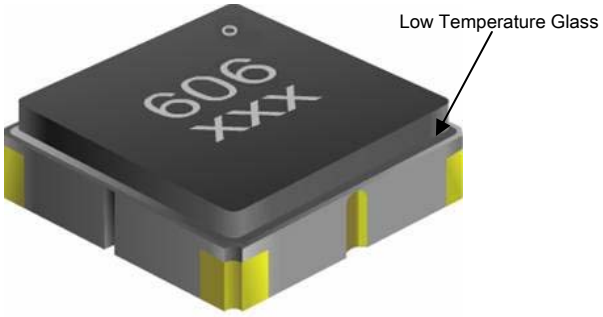

Figure 9

'606' is the laser marking designating the product type, and 'xxx' is the lot number

Note:

- When soldering manually or repairing via soldering iron for the DTOS, the time must be limited to less than 10 seconds and the temperature must not exceed 275℃. If a heat gun is used, the time must be limited to less than 10seconds and the temperature must not exceed 270℃
- Avoid bending the PCB after the sensor assembly

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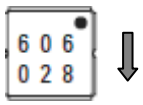
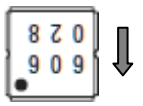
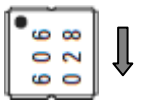
Orientation/Shake Characteristics

Orientation	State Bits OR [1,0]
	00
	01
	10
	11

Gravity direction

DTOS Output state response to orientation

If the sensor is rotated past the 45 degree threshold, the orientation bits will change only if the sensor stays in the same state for a defined period of time. If the sensor crosses back before this time period, the orientation bits remain unchanged. This is to prevent dithering of the orientation state. Four user programmable hysteresis time periods are available: 160, 320, 640 and 1280ms.

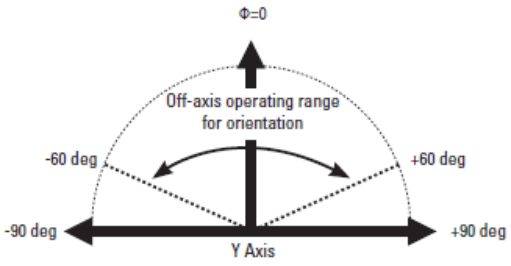


Figure 11

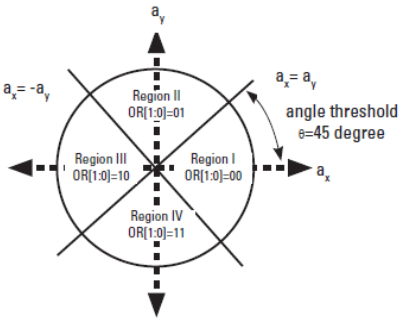


Figure 12

DTOS can detect orientation changes with up to 60 degrees of off-axis tilt

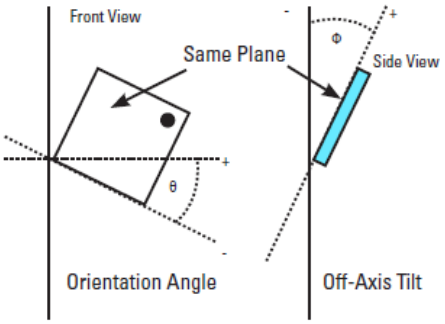


Figure 10

DTOS Shake Detection

Shake and shake direction are orthogonal to screen orientation. An interrupt pin (INT) is set high and must be cleared by the MCU via the I^2C interface. Four user programmable thresholds are available: 0.5g, 1g, 1.5g and 2g, , and these can be applied either to the X-axis, Y-axis, or both axes.

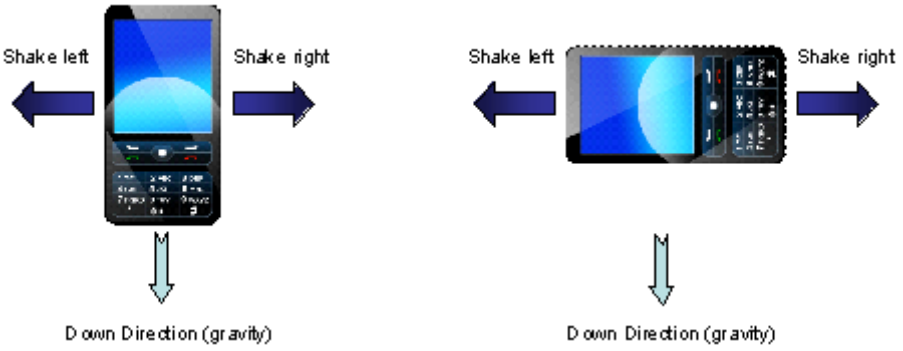


Figure 13

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DTOS I²C Interface

A slave mode I²C interface, capable of operating in standard or fast mode, is implemented on the DTOS. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bi-directional communication between master and slave devices. A master (typically a microprocessor) initiates all data transfers to and from the device, and generates the SCL clock that synchronizes the data transfer. The SDA pin on the DTOS operates both as an input and an open drain output. Since the DTOS only operates as a slave device, the SCL pin is always an input. There are external pull-up resistors on the I²C bus lines. Devices that drive the I²C bus lines do so through open-drain n-channel driver transistors, creating a wired NOR type arrangement.

Data on SDA is only allowed to change when SCL is low. A high to low transition on SDA when SCL is high is indicative of a START condition, whereas a low to high transition on SDA when SCL is high is indicative of a STOP condition**.** When the interface is not busy, both SCL and SDA are high. A data transmission is initiated by the master pulling SDA low while SCL is high, generating a START condition. The data transmission occurs serially in 8 bit bytes, with the MSB transmitted first. During each byte of transmitted data, the master will generate 9 clock pulses. The first 8 clock pulses are used to clock the data, the 9th clock pulse is for the acknowledge bit. After the 8 bits of data are clocked in, the transmitting device releases SDA, and the receiving device pulls it down so that it is stable low during the entire 9th clock pulse. By doing this, the receiving device "acknowledges" that it has received the transmitted byte. If the slave receiver does not generate an acknowledge, then the master device can generate a STOP condition and abort the transfer. If the master is the receiver in a data transfer, then it must signal the end of data to the slave by not generating an acknowledge on the last byte that was clocked out of the slave. The slave must release SDA to allow the master to generate a STOP or repeated START condition.

The master initiates a data transfer by generating a START condition. After a data transmission is complete, the master may terminate the data transfer by generating a STOP condition. The bus is considered to be free again a certain time after the STOP condition. Alternatively, the master can keep the bus busy by generating a repeated START condition instead of a STOP condition. This repeated START condition is functionally identical to a START condition that follows a STOP. Each device that sits on the I²C bus has a unique 7-bit address.

The first byte transmitted by the master following a START is used to address the slave device.

The first 7 bits contain the address of the slave device, and the 8th bit is the R/W* bit (read = 1, write = 0; the asterisk indicates active low, and is used instead of a bar). If the transmitted address matches up to that of the DTOS, then the DTOS will acknowledge receipt of the address, and prepare to receive or send data.

If the master is writing to the DTOS, then the next byte that the DTOS receives, following the address byte, is loaded into the address counter internal to the DTOS. The contents of the address counter indicate which register on the DTOS is being accessed. If the master now wants to write data to the DTOS, it just continues to send 8-bit bytes. Each byte of data is latched into the register on the DTOS that the address counter points to. The address counter is incremented after the transmission of each byte.

If the master wants to read data from the DTOS, it first needs to write the address of the register it wants to begin reading data from to the DTOS address counter. It does this by generating a START, followed by the address byte containing the DTOS address, with R/W* = 0. The next transmitted byte is then loaded into the DTOS address counter. Then, the master repeats the START condition and re-transmits the DTOS address, but this time with the R/W* bit set to 1. During the next transmission period, a byte of data from the DTOS register that is addressed by the contents of the address counter will be transmitted from the DTOS to the master. As in the case of the master writing to the DTOS, the contents of the address counter will be incremented after the transmission of each byte. The protocol for multiple byte reads and writes between a master and a slave device is depicted in

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Figure 14.

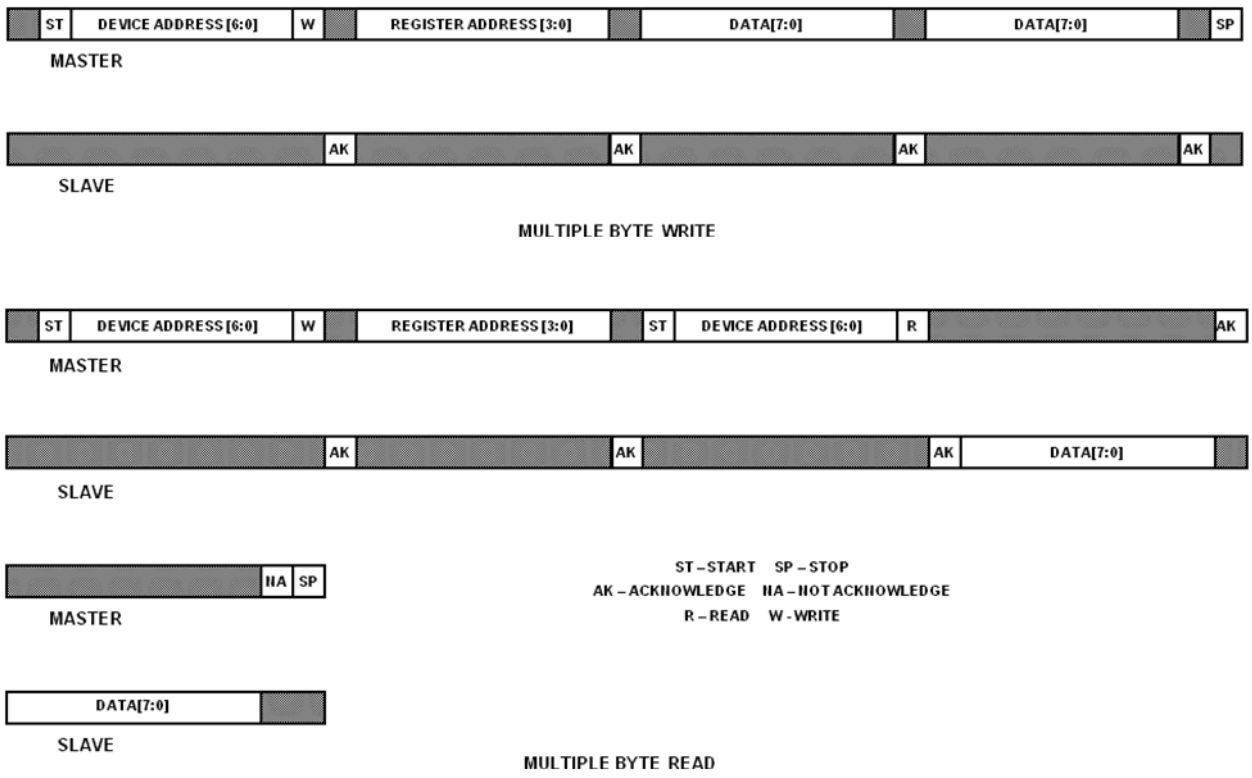

Figure 14

The 7-bit I^{2}C address for DTOS is set as 0010110b.

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User Register Summary

Address	Name	Definition	Access	Default
$00	XOUT	8-bit x-axis acceleration output	read	00000000
$01	YOUT	8-bit y-axis acceleration output	read	00000000
$02	STATUS	orientation and shake status	read	00000000
$04	DETECTION	Power down, orientation and shake detection parameters	write	00000000
$08	CHIP_ID	Chip ID of MXC6226XU	read	xx100110

The registers available to the user on the DTOS are summarized in the table above. Each register contains 8 bits.

$00: XOUT – 8-bit x-axis acceleration output (read only)

D7	D6	D5	D4	D3	D2	D1	D0
XOUT[7]	XOUT[6]	XOUT[5]	XOUT[4]	XOUT[3]	XOUT[2]	XOUT[1]	XOUT[0]

8-bit x-axis acceleration output. Data in 2's complement format with range of -128 to +127.

$01: YOUT – 8-bit y-axis acceleration output (read only)

D7	D6	D5	D4	D3	D2	D1	D0
YOUT[7]	YOUT[6]	YOUT[5]	YOUT[4]	YOUT[3]	YOUT[2]	YOUT[1]	YOUT[0]

8-bit y-axis acceleration output. Data in 2's complement format with range of -128 to +127.

$02: STATUS – orientation and shake status register (read only)

D7	D6	D5	D4	D3	D2	D1	D0
INT	SH[1]	SH[0]	TILT	ORI[1]	ORI[0]	OR[1]	OR[0]

OR[1:0] is a 2-bit indication of the device orientation, according to the following scheme (also shown visually in Figure 10): OR[1:0] = 00 – device is vertical in upright orientation; 01 – device is rotated 90 degrees clockwise; 10– device is vertical in inverted orientation; 11 – device is rotated 90 degrees counterclockwise. The bits OR[1:0] are indicative of "long-term" orientation. The orientation is determined by measuring the signs of the quantities ax – ay, and ax + ay, as shown in Figure 12. The orientation measurement is ignored for any samples in which the magnitudes of ax and ay are both less than 3/8 g (for example, during a free-fall event). In order for a new value of OR[1:0] to be written to the STATUS register, a valid measurement of the new orientation must be measured a consecutive number of times determined by the setting of bits ORC[1:0] in the DETECTION register. This provides a low-pass filtering and hysteresis effect that keeps a display from flickering near orientation boundaries.

ORI[1:0] is the instantaneous device orientation. It follows the same scheme as OR[1:0], except that it is updated every time a valid orientation measurement is made, not subject to the same low-pass filtering as OR[1:0].

TILT is an indication of whether there is enough acceleration signal strength to make a valid orientation measurement. If TILT = 0, the orientation measurement is valid, if TILT = 1, then the orientation measurement is invalid. TILT is updated every measurement cycle.

SH[1:0] indicate whether a shake event has taken place, and if so, its direction. Shake can only be detected in a direction perpendicular to the vertical

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orientation of the device. When an acceleration perpendicular to the device orientation (ax for OR[1:0] = 01 or 11; ay for OR[1:0] = 00 or 10) is sensed that has a magnitude greater than the value set by bits SHTH[1:0] in the DETECTION register, then shake detection begins. For a shake event to be written to SH[1:0], the perpendicular acceleration must again exceed the magnitude set by SHTH[1:0] but with the opposite sign (if bit SHM = 0 in the DETECTION register), or just reverse its sign (if bit SHM = 1 in the DETECTION register). The above mentioned second acceleration events must occur within a certain amount of time, set by SHC[1:0] in the DETECTION register, of the original breaking of the threshold.

If a shake is determined to have occurred, then the direction of the shake can be determined by the signs of the accelerations. The shake status is indicated as shown in the following table:

SH[1]	SH[0]	Comment
0	0	no shake event
0	1	shake left
1	0	shake right
1	1	undefined

INT is the interrupt bit. Setting this bit high will cause the INT pin to output a high level. The INT bit will be set whenever either (1) The orientation, as indicated by bits OR[1:0] changes, or (2) A shake event occurs. The microprocessor can then service the interrupt by reading the STATUS register. Once a shake event occurs, no new shake events will be recorded until the interrupt has been serviced, although the orientation bits will continue to be updated. The INT bit is cleared by reading the STATUS register.

$04: DETECTION – orientation and shake detection parameters (write only)

D7	D6	D5	D4	D3	D2	D1	D0
PD	SHM	SHTH[1]	SHTH[0]	SHC[1]	SHC[0]	ORC[1]	ORC[0]

PD = 1 powers down the DTOS to a non-functional low power state with a maximum current drain of 1 uA.

ORC[1:0] sets the orientation hysteresis time period, which is the time period of consecutive valid new instantaneous orientation measurements that must be made before a new orientation value is written into bits OR[1:0] in the STATUS register. The "long-term" orientation change is set by ORC[1:0] as follows: 00 – 160ms, 01 – 320ms, 10 – 640ms, 11 – 1280ms nominally.

SHC[1:0] sets the shake events time window, which determines the time window allowed between the first shake event (perpendicular acceleration exceeding the threshold set by SHTH[1:0]) and the second shake event (acceleration breaking the threshold with opposite sign, SHM = 0, or just reversing sign, SHM = 1). The time window is set by SHC[1:0] as follows: 00 – 80ms, 01 – 160ms, 10 – 320ms, 11 – 640ms nominally.

SHTH[1:0] sets the shake threshold that the perpendicular acceleration must exceed to trigger the first shake event. The settings for SHTH[1:0] are: 00 - 0.5 g, 01 – 1.0 g, 10 – 1.5 g, 11 – 2.0 g.

SHM is the shake mode bit. If SHM = 0, then for a shake to be detected, and written to SH[1:0] in the STATUS register, the second shake event must break the threshold set by SHTH[1:0] with the opposite sign of the first shake event, within the time window set by SHC[1:0]. If SHM = 1, then the second shake event must just have the opposite sign of the first shake event within the time window set by SHC[1:0].

$08 (6LSB): CHIP_ID – Chip ID of MXC6226XU (read only)

D7	D6	D5	D4	D3	D2	D1	D0

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ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]
X	X	1	0	0	1	1	0

Device identification register (6LSB) which is set as 26h for MXC6226XU.

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Sensitivity/Offset Distribution (@ 25℃, VDD = 3V)

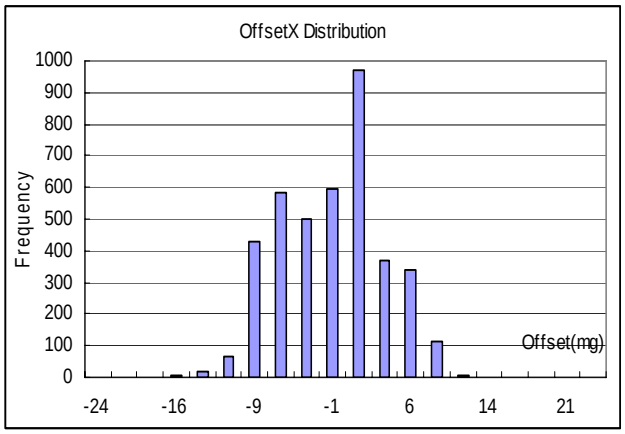

Figure 15

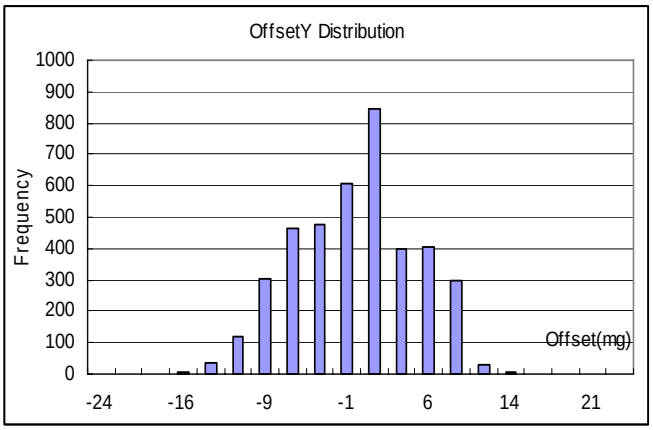

Figure 16

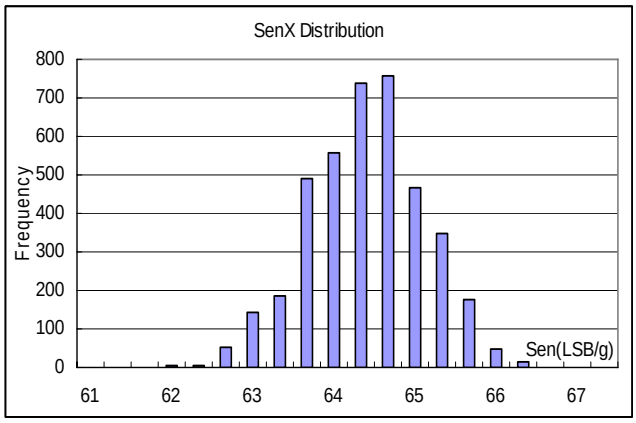

Figure 17

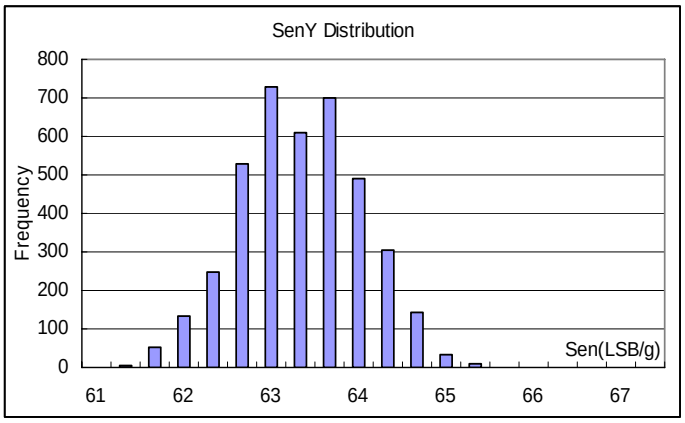

Figure 18

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Over Temperature Characteristics

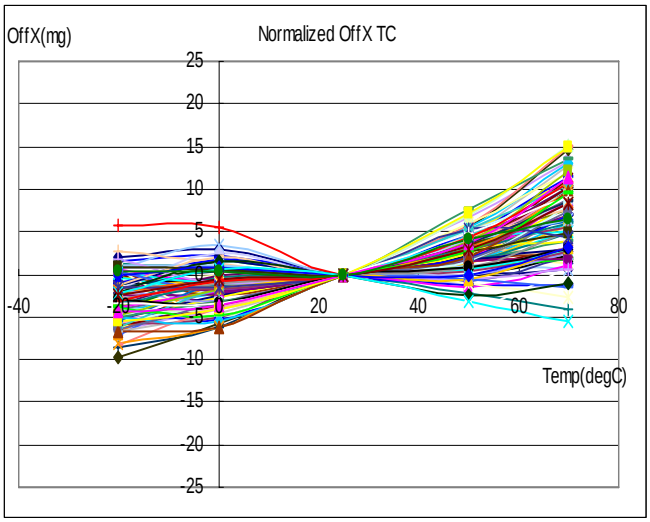

Figure 19

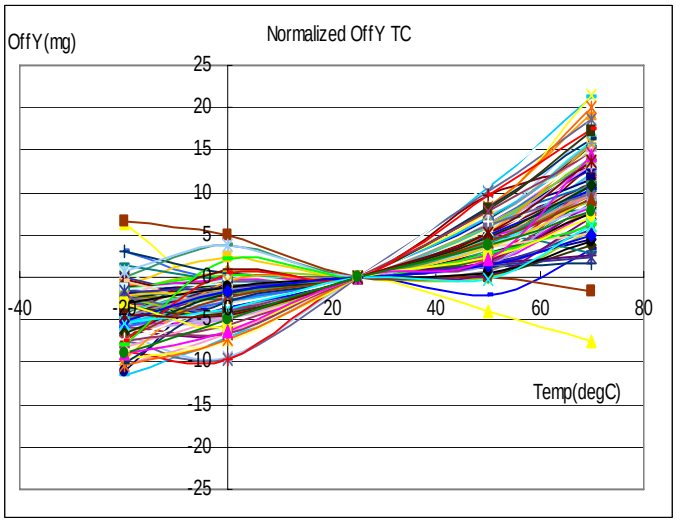

Figure 20

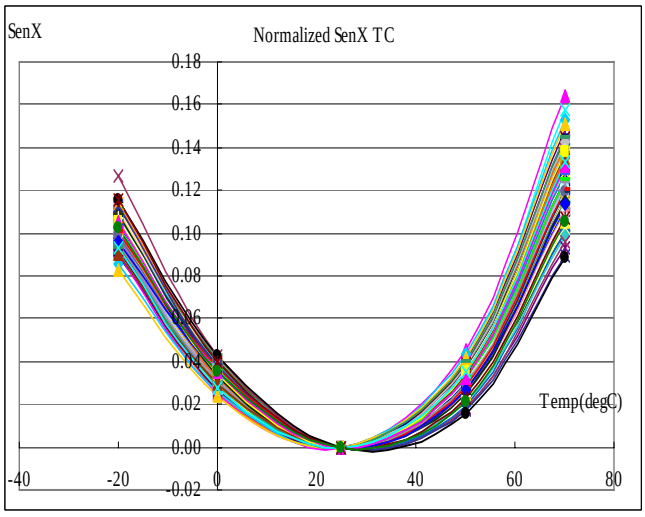

Figure 21

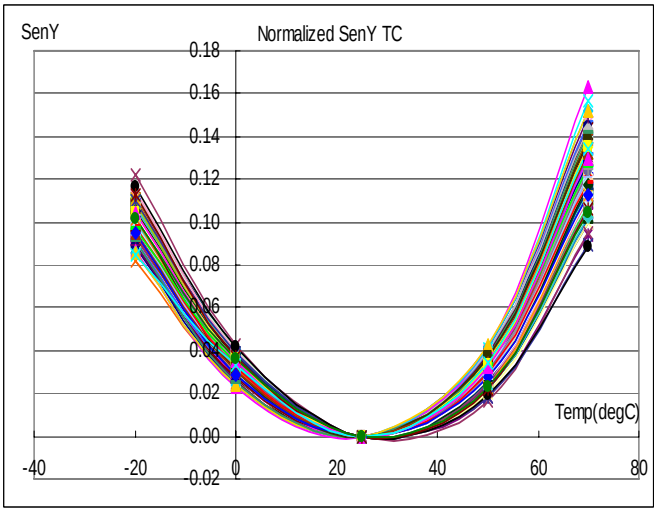

Figure 22

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Device Marking Illustration

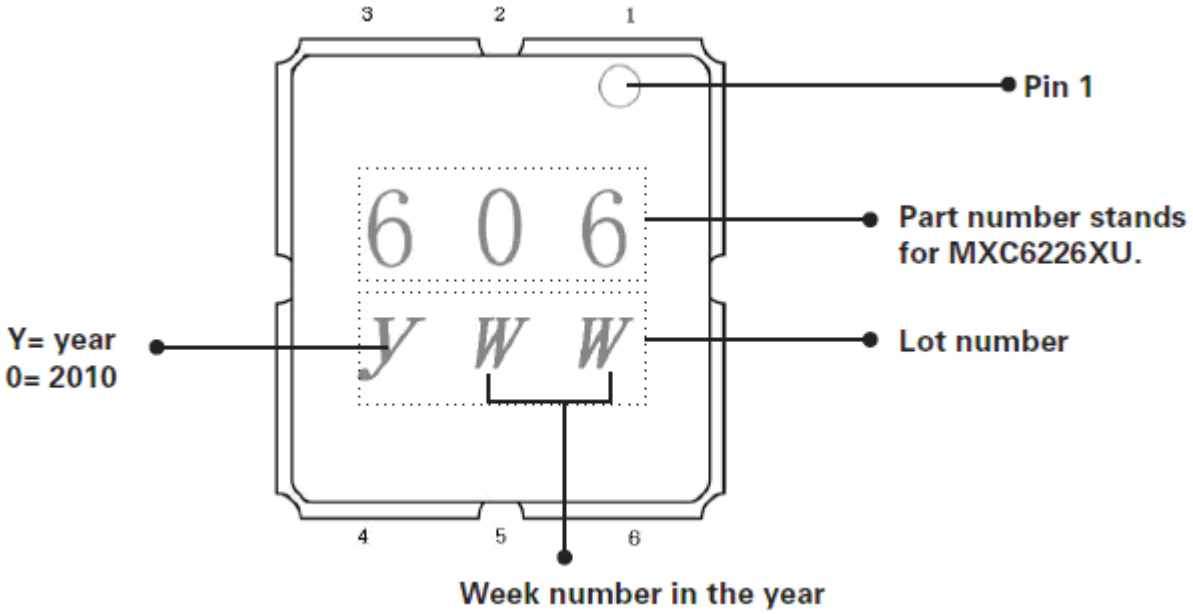

Figure 23

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